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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,470	11/20/2001	Akihiro Kirisawa	03830045AA	8763

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EXAMINER	
KENDALL, CHUCK O	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,470	KIRISAWA, AKIHIRO	
	Examiner	Art Unit	
	Chuck Kendall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/30/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application fled 12/15/04.

2. Claims 1 - I 5 are pending.

Claim Rejections - 35 USC 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 - 12, & 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Warmink USPN 6,301,709 B1.

Regarding claim 1, a program updating system having a communication function comprising:

a first processor which operates by referring to a program stored therein (FIG. 1, see FIRST CIRCUIT PACT, 20 and associated text); and

a second processor which executes update of said program by using said communication function with an external unit, and executes an update control of said program when a fault of said first processor is detected (FIG. 1, see SECOND CIRCUIT PACT, 30, and associated text for updating see, 4:12 – 17, see checks the state of the signal switch for current software (fault detection)).

Regarding claim 2, the program updating system having the communication function according to claim 1, wherein said second processor transmits a reset signal to said first processor for every predetermined cycles, and monitors a response pulse

which is transmitted from said first processor in response to said reset signal, and transmits a compulsory reset signal to said first processor when said response pulse can not be detected within a predetermined period (3:30 - 55, see reset and see answering request, also see 2: 65 -67, for circuit pack which did not receive signal (for pulse not detected).

Regarding claim 3, the program updating system having the communication function according to claim 2, further comprising;

an activation pulse generating circuit which generates an activation pulse to activate said second processor (4:20 – 25), wherein said second processor starts transmitting of said reset signal in response to said activation pulse outputted from said activation pulse generating circuit (2:35 -45, see receiving request and answering them).

Regarding claim 4, the program updating system having the communication function according to claim 3, further comprising:

a buffer which transiently stores said program for executing said update control, wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program in said buffer is completed (1 : 53 - 57, see memory storage area).

Regarding claim 5, the program updating system having the communication function according to claim 1, further comprising..

an activation pulse generating circuit which generates an activation pulse to activate said second processor, wherein said second processor starts transmitting of said reset signal in response to said activation pulse outputted from said activation pulse generating circuit (2: 33 -35, for activation pulse see receiving reset and start).

Regarding claim 6, the program updating system having the communication function according to claim 5, further comprising:

a buffer which transiently stores said program for executing said update control, wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program to said buffer is completed (1:55 - 65).

Regarding claim 7, the program updating system having the communication function according to claim 1, further comprising:

a buffer which transiently stores said program for executing said update control, wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program to said buffer is completed (1 :55 - 65).

Regarding claim 8, the program updating system having the communication function according to claim 2, further comprising;

an activation monitoring circuit which generates an activation pulse to activate said second processor and monitors transmission of an activation response pulse which is outputted from said second processor in response to said activation pulse, wherein said activation monitoring circuit transmits a compulsory reset signal to said second processor when said activation response pulse can not be detected within the predetermined period (3:30 - 55, see
reset and see answering request, also see 2:30 - 37, and 65 - 67, for circuit pack which did not receive signal (for pulse not detected).

Regarding claim 9, the program updating system having the communication function according to claim 8, further comprising;

a buffer which transiently stores said program for executing said update control, wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program to said buffer is completed (1:55 - 65).

Regarding claim 10, the program updating system having the communication function according to claim 1, further comprising:

an activation monitoring circuit which generates an activation pulse to activate said second processor and monitors transmission of an activation response pulse outputted from said second processor in response to said activation pulse, wherein said activation monitoring circuit transmits a compulsory reset signal to said second processor when said activation response pulse can not be detected within the

predetermined period (3:30 - 55, see reset and see answering request, also see 2:30 - 39 and 65 - 67, for circuit pack which did not receive signal
(for pulse not detected).

Regarding claim 11, the program updating system having the communication function according to claim 10, further comprising;

a buffer which transiently stores said program for executing said update control, wherein said second processor transfers said program stored in said buffer to said first processor, after an operation of storing said program to said buffer is completed (1: 45 - 65).

Regarding claim 12, which recites the method version of claim 1, see rationale as Previously discussed above.

Regarding claim 15, the program updating method using the communication function according to claim 12, further comprising; providing an activation control circuit which controls activation and a stop of said second processor, wherein said second processor transmits an activation response pulse to said activation control circuit for every predetermined cycles, and said activation control circuit executes a stop control of said second processor, when said activation response pulse can not be detected within a predetermined period (3:30 - 55, see reset and see answering request, also see 2:30 - 37, and 65 - 67, for circuit pack which did not
receive signal (for pulse not detected).

Claim Rejections - 35 USC 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 13, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Warmink USPN 6,301,709 B1 as applied in claim 12, in view of Ghori et al. USPN 5,884,091.

Regarding claim 13, Warmink discloses all the claimed limitations as applied in claim 12 above. Warmink doesn't explicitly disclose wherein said second processor transfers said program obtained by using said communication function to said first processor, during a stop of said first processor, although Warmink does mention a master and slave circuit as well as transmitting resetting signals (2:33 - 45). Ghori discloses in an analogous art disabling the processor during a RESET at which time the master processor is being designated as the active processor (8:43 - 45). Therefore it would have been obvious to one of ordinary skills in the art at the time invention was made to combine Warmink and Ghori because, stopping or disabling the processor after a reset would enable more efficient configuring during updating.

Regarding claim 14, the program updating method using the communication function according to claim 13, further comprising;

providing an activation control circuit which controls activation and a stop of said second processor, wherein said second processor transmits an activation response pulse to said activation control circuit for every predetermined cycles, and said activation control circuit executes a stop control of said second processor, when said activation response pulse can not be detected within a predetermined period (Warmink, 3:30 - 55, see reset and see answering request, also see 2:30 - 37, and 65 - 67, for circuit pack which did not receive signal (for pulse not detected)).

Response to Arguments

Applicant's arguments filed 12/15/2004 have been fully considered but they are not persuasive. Applicant argues on page 9 of Applicant's response as dated above

that Warmink does not teach or suggest fault detection, and also does not suggest the capability to upgrade software in a processor that fails to communicate.

Examiner disagrees, Warmink does disclose teach this limitation, In 4:12 – 17, Warmink teaches checking the state of the signal switch for current software (fault detection)) and depending on the status of the software i.e. whether it's current or older it then implements the upgrade, Examiner believes this to be equivalent to Applicant's claimed limitations in claim 1.

Applicant also argues in claim 2, that prior art does not teach transmitting a compulsory reset signal when response cannot be detected.

Responding, Warmink discloses transmitting data when signal pack did not receive signal (response not detected) (2:62 – 67) as interpreted by Examiner, this teaches Applicant's above claimed limitation.

Applicant also argues Warmink does not teach " activating pulse that causes a circuit pack or processor to transmit a reset signal".

Responding Warmink discloses in 4:20 – 25, when a hardware signal is off, then no update occurs and nothing further occurs until the next reset signal. Examiner interprets this to be equivalent to Applicant's claim.

Regarding arguments in claim 8, see claim 2 as previously discussed above in reference to "pulse not detected".

Regarding Warmink not teaching a stop control when response is not detected as claimed in 14 and 15, Ghori is provided as secondary art to teach that limitation. Ghori discusses disabling (stop) during reset (8:43 – 45).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-272-3698. The examiner can normally be reached on 10:00 am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ck.

TUAN DAM
SUPERVISORY PATENT EXAMINER